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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,579	10/23/2003	Noriyuki Miura	MAE 296	5973

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EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/690,579	MIURA, NORIYUKI	
	Examiner	Art Unit	
	Dana Farahani	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Maeda et al., hereinafter Maeda (US Patent 6,414,353).

Regarding claims 1 and 9, Maeda discloses in figure 1 a MOS transistor having an insulating layer 2 and a silicon layer 3 (or SOI film, as it is called in claim 1) which is disposed on a substrate 1; gate insulator 19 disposed on the silicon layer; a gate electrode 20 which is made of p-type polysilicon, disposed on the semiconductor substrate so that the gate insulator is disposed between the gate electrode and the semiconductor substrate; a channel region formed in the silicon layer, which is disposed under the gate electrode; and a source and a drain 4 and 6,

respectively, formed in the silicon layer and being adjacent to the channel region; wherein conductivity types of the channel region, the source and the drain are n-type.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda as applied to claims 1and 9 above, and further in view of Tsukii et al., hereinafter Tsukii (US Patent 4,772,858).

Maeda substantially discloses the claimed invention, as discussed above, except for a channel impurity of approximately 3 * 10 to the power of 18 (10^18).

Tsukii discloses an amplifier circuitry wherein a channel concentration of approximately 3*10^18 is formed in the individual field effect transistors of the circuit (see column 7, line 30). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the channel of the Maeda's transistor with this amount of concentration in order to make the transistor applicable in an integrated circuit strucutre such as the amplifier circuitry of the Tsukii reference.

5. Claims 4, 5, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda as applied to claims 1 and 9 above, and further in view of Stein et al., hereinafter Stein (US Patent 4,021,787).

Maeda substantially discloses the claimed invention, as discussed above, except for the gate insulator being 2 nm.

Stein discloses a MOS transistor wherein the gate insulator thickness is 2 nm (see column 1, line 55) so the transistor can be used in a memory circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the thickness of the gate insulator of the Maeda structure 2 nm in order to make the transistor applicable in an integrated circuit strucutre such as a memory circuit. Although, the Maeda reference does not disclose the silicon layer 30 has a 20 nm thickness, it would have been obvious to make that layer 20 nm to adjust the characteristics of the device. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990) for the proposition that where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, Applicant must show that the chosen dimensions are critical.

6. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda as applied to claims 1 and 9 above, and further in view of Yamada (US Patent 5,923,070).

Maeda substantially discloses the claimed invention, as discussed above, except for the source and drain having an impurity concentration of not less than approximately 1*10^21.

Yamada discloses a MOS transistor with that amount of impurity concentration in the source/drain (see column 7, line 55-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the drain and source of the MOS transistor of the Maeda reference with this amount of impurity, in order to adjust the drain current to a value that corresponds to that impurity concentration, and make the transistor applicable in a circuitry which needs that corresponding value of the drain current.

7. Claims 7, 8, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda as applied to claims 1 and 9 above, and further in view of Kato et al., hereinafter Kato (US Patent 5,793,678).

Maeda substantially discloses the claimed invention, as discussed above, except for explicitly disclosing the length of the channel region being approximately 0.15 Microns. However, Maeda teaches that the channel length can be varied to a value for adjusting the saturation of the gate threshold voltage (see column 20, lines 25-29).

Kato discloses at column 2, line 5 a MOS transistor with a channel length of 0.15 Micron. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the channel length of the Maeda's transistor about this length, in order to adjust the saturation of the gate threshold voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
PRIMARY EXAMINER